DISCUSSION OF THE AMENDMENT

Claims 1, 2, 5-24, and 27-30 are active in the present application. Claims 29 and 30 are new claims. Support for new Claim 29 is found in the paragraph bridging pages 27 and 28. Support for new Claim 30 is found on page 26, lines 18-19.

No new matter is added.

REMARKS

Applicants thank Examiner Arancibia for discussing this case with Applicants' U.S. representative on December 29, 2008. During the discussion it was argued that it would not be obvious to use the annealing step (e.g., the heating step) of the <u>Falster</u> patent in place of the gettering step of the <u>Lawrence '567</u> patent. It was pointed out that the <u>Falster</u> method is substantially different from the <u>Lawrence</u> method because the <u>Falster</u> method treats a silicon wafer having only small amounts of copper present on the surface whereas the <u>Lawrence</u> method requires the removal of substantially greater amounts of copper impurities that are under the wafer surface.

Applicants thank the Office for acknowledging that the rejection set forth in the Office Action of April 2, 2008 was not supportable. The Office now rejects the claims as obvious over a combination of <u>Lawrence '567</u> (US 3,923,567); <u>Falster</u> (US 6,100,167) and <u>Lawrence '875</u> (US 5,622,875). Applicants submit the rejection is not legally supportable at least for the reason that the Office failed to set forth a *prima facie* case of obviousness.

The Office relies on <u>Lawrence '567</u> as evidence that conventional methods of treating silicon wafers include film removal, heating/removal, polishing and cleaning processes (see section no. 3 on page 2 of the October 22 Office Action). The Office admits that <u>Lawrence '567</u> does not teach several of the features recited in present Claim 1. For example, the Office acknowledges that <u>Lawrence '567</u> does not disclose the heating step of the heating/removal process recited in present Claim 1. The Office relies on <u>Falster</u> as evidence that it would be obvious to modify the process of <u>Lawrence '567</u> with the <u>Falster</u> heating/removal process.

At the outset is must be noted that the presently claimed invention ("a method of reclaiming silicon wafers") is substantially different from the method disclosed in <u>Falster</u>. For example, <u>Falster</u> discloses a process for removing copper from boron doped silicon wafers

(see the title of <u>Falster</u>). The copper removed in the <u>Falster</u> process is copper that has been inadvertently added to a wafer during polishing (see column 1, lines 31-50 of <u>Falster</u>). The amount of copper on the surface of the <u>Falster</u> wafer is on the order of 10¹¹ atoms/cm² (see Figure 2 of <u>Falster</u>), substantially less than the amount of copper present on a wafer undergoing reclamation, e.g., 10¹⁴ atoms/cm² (see Figure 3 of the present specification).

Applicants submit that those of skill in the art would not turn to <u>Falster</u> as inspiration for arriving at the presently claimed invention in view of the fact that the <u>Falster</u> process is one oriented towards treating polished silicon wafer surfaces having ultralow amounts of copper impurity whereas the presently claimed invention treats silicon wafers having copper in an amount that is about 1,000 times greater than the amount of copper present on the Falster wafers.

In support of its assertion of obviousness, the Office asserts that the paragraph bridging columns 1 and 2 of <u>Falster</u> show that one of ordinary skill in the art would have been motivated to substitute the gettering step disclosed in the <u>Lawrence '567</u> patent with the Falster annealing step.

Applicants submit that the Office's logic in this regard is faulty. First, the <u>Lawrence</u> '567 process uses a gettering step in combination with an etching step. The gettering serves to bring impurities to the surface of the <u>Lawrence</u> '567 silicon wafer. The etching then removes portions of the silicon wafer containing the impurities (see column 4, lines 6-51 of <u>Lawrence</u> '567). Thus, gettering and etching go hand-in-hand in the <u>Lawrence</u> '567 process. It would make no sense to carry out the etching step of <u>Lawrence</u> '567 in the absence of the gettering step because no purpose would be served other than the removal of portions of the silicon wafer.

This point is important because one of ordinary skill in the art would not simply substitute the annealing step of <u>Falster</u> for the gettering step of <u>Lawrence '567</u>. Instead, as

explained in <u>Falster</u>, one of skill in the art would substitute the gettering/chemical etching of <u>Lawrence '567</u> with the annealing/cleaning of <u>Falster</u>. <u>Falster</u> makes it absolutely clear that after annealing (e.g., heating) is carried out, a silicon wafer is subjected to an SC-1 or SC-2 "cleaning step" (see column 4, lines 26-38 of <u>Falster</u>). <u>Falster</u> does not suggest that any etching should be carried out after annealing. In fact, to the contrary, <u>Falster</u> cautions that exposure to the SC-1 solution should be for only short periods of time in order to avoid etching, pitting and roughening (see column 4, lines 56-64 of <u>Falster</u>). This follows further from the fact that the <u>Falster</u> process is one for removing adventitious amounts of copper introduced to the wafer surface during polishing without ruining the wafer's surface polish.

Any asserted modification of <u>Lawrence '567</u> using <u>Falster</u> would require substitution of the gettering/etching of <u>Lawrence '567</u> with the annealing/cleaning of <u>Falster</u>. As disclosed in <u>Falster</u>, gettering/annealing is necessarily carried out in a manner to avoid excessive etching, pitting or roughening. If the Office was correct in asserting that one of skill in the art would modify <u>Lawrence '567</u> according to <u>Falster</u>, the resultant process would be one that did not include etching, contrary to the claimed invention.

As explained at length in the Amendment filed in the present application on July 3, 2008, etching the surface of a silicon wafer to a depth of about 1 µm is a requirement of the presently claimed invention. The combination of <u>Lawrence '567</u> and <u>Falster</u> is directly contradictory to such a requirement because, as pointed out above, the substitution of the gettering/etching of <u>Lawrence '567</u> with the annealing/cleaning of <u>Falster</u> would, according to <u>Falster</u>, be carried out in a manner such that etching is not included.

For at least this reason the Office's assertion that the presently claimed subject matter is obvious over the combination of <u>Lawrence '567</u> and <u>Falster</u> is not supportable and should be withdrawn.

The Office admits that <u>Lawrence '567</u> and <u>Falster</u> do not "teach that the chemical removal step comprises etching the silicon wafer ... to a depth of 1 µm" (see paragraph 4 of the October 22 Office Action). It thus appears that the Office is in agreement that the combination of <u>Lawrence '567</u> and <u>Falster</u> makes no sense.

In an effort to make up for this inherent contradiction in the rejection the Office further cites to <u>Lawrence '875</u> for disclosure of a method of treating a silicon wafer that includes etching. As already pointed out above, it makes no sense to include chemical etching in a process of <u>Lawrence '567</u> as modified by <u>Falster</u> for the reason that <u>Falster</u> teaches away from such etching. For this reason alone the combination of <u>Lawrence '567</u>, <u>Falster</u>, and <u>Lawrence '875</u> does not make sense and the rejection should be withdrawn.

The Office puts forth a further incorrect basis for asserting that one of ordinary skill in the art would be motivated to modify <u>Lawrence '567</u> and/or <u>Falster</u> in the manner of <u>Lawrence '875</u>. The Office asserts the following:

It would have been obvious to one of ordinary skill in the art to further modify the method taught by the combination of Lawrence ['567] and Falster et al. to have the same chemical removal solution comprise KOH, as an art-recognized suitable etchant as taught by US '875 for that purpose, and to etch the silicon wafer to a depth of at least 1 micron, in order to, as taught by US '875 (Column 8, Lines 13-31), remove impurities from the wafer and to remove an unwanted top surface layer of silicon having considerable crystalline strain.

See the last paragraph on page 4 of the October 22 Office Action.

Applicants submit that the Office's basis set forth in the above-quoted text is contradictory to the express disclosure of the cited art. For example, the Office asserts that the art discloses using chemical etching to remove impurities from the wafer. Present Claim 1 recites removing a portion of a top surface of a silicon wafer. Although the Office asserts that Lawrence '875 discloses that etching provides a manner in which impurities may be removed from a wafer, Applicants point out that Lawrence '875 discloses only that impurities

may be removed from the <u>edge</u> of a silicon wafer. In fact, <u>Lawrence '875</u> discloses the following:

Still another advantage is that the etching removes impurities from the wafer edge.

See column 8, lines 17-18 of Lawrence '875.

<u>Lawrence</u> does not disclose that impurities are removed from a top surface of a silicon wafer. To the contrary, <u>Lawrence</u> discloses that silicon having crystalline strain is removed from a top surface layer of the silicon wafer (see column 8, lines 15-18). Applicants submit that, at best, <u>Lawrence</u> discloses that etching is useful for removing crystalline strain imparted by certain grinding steps. Applicants submit that those of ordinary skill in the art could have no basis to extend such a teaching in the manner asserted by the Office in view of the express disclosure of the cited art.

Therefore, the Office's basis for asserting that one of ordinary skill in the art would modify <u>Lawrence '567</u> and/or <u>Falster</u> in the manner of <u>Lawrence '875</u> is not supportable and the rejection should be withdrawn.

Applicants draw the Office's attention to new dependent Claim 29 which recites a step of treating the silicon wafer with at least one of an SC1 and an SC2 liquid before the chemical process of Claim 1. Applicants submit that the art relied on by the Office nowhere discloses or suggests the sequence of steps recited in new dependent Claim 29. In fact, at best, <u>Falster</u> discloses a step of treating a silicon wafer with an SC1 or SC2 liquid only after a silicon wafer has been subjected to annealing, not before the silicon wafer has been subjected to heating.

Applicants thus submit that dependent Claim 29 is further patentable over the art of record.

Applicants further draw the Office's attention to new dependent Claim 30 which requires that the silicon wafer is contacted with only an alkali solution in the chemical process of Claim 1. Applicants submit that new dependent Claim 30 excludes the processes of, for example, <u>Lawrence '567</u> and <u>Falster</u> and thus the combination of cited art does not render the subject matter of new dependent Claim 30 obvious.

The Amendment filed on the present case on July 2, 2008 included an explanation of Applicants' data showing that treating a silicon wafer in the manner recited in Claim 1 provides a silicon wafer having a substantially produced amount of copper impurities. The Office provided a response in section no. 8 on pages 10-11 of the October 22 Office Action. The Office asserts that because the cited art suggests the claimed invention, one of ordinary skill in the art would expect the resulting process to exhibit the results demonstrated by Applicants.

If the Office's assertion and understanding of the law were correct it would never be possible to demonstrate unexpected results. This is clearly an incorrect statement of the law. Applicants draw the Office's attention to MPEP § 716.02(e) for a discussion of the merits of an applicant's showing of unexpected results.

Here, Applicants have demonstrated that treating a silicon wafer with the heating/removal step of the present claims provides a silicon wafer having a substantially reduced amount of copper. Applicants provided numerous comparative examples demonstrating the amount of copper left in a silicon wafer after treatment of the silicon wafer with other treatment solutions such as HF/H₂O₂. These results are depicted in an easy to understand format in Figure 3. It is readily evident from Figure 3 that the amount of copper remaining after treatment with the etching solution of the present claims is only a small fraction of the amount of copper remaining after treatment of a silicon wafer with an acidic, e.g., HF-containing, liquid. If the Office's assertion were correct that one of ordinary skill in

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the art would obviously have substituted an alkaline cleaning step for an acid cleaning step,

then one of ordinary skill in the art would have expected equivalent results to be obtained,

e.g., equivalent copper removal.

Applicants have shown that this is not the case. Applicants' data show that the

presently claimed invention provides a silicon wafer that is substantially improved to the

silicon wafers obtained by using treatment processes that contact a silicon wafer surface with

treatment liquids other than the treatment liquid recited in the present claims.

Applicants submit that the data of the original specification, e.g., as embodied in

Figure 3, are probative of the patentability of the presently claimed invention. The Office's

refusal to give Applicants' data consideration and support of patentability is legal error.

Applicants thus submit that the presently claimed invention is thus further patentable over the

art of record in view of Applicants' data set forth in the original specification.

For the reasons discussed above in detail, Applicants submit the rejections are not

supportable and should be withdrawn. Applicants request withdrawal of the rejections and

the allowance of all now-pending claims.

Respectfully submitted,

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